IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1-3. (Cancelled)

4. (Currently Amended) An intermediate semiconductor device fabrication structure comprising: a plurality of electronic chip components, each having all electrodes formed on one surface thereof, side walls thereof being covered with a protective material, and wherein ~~there is substantially no protective material located on~~ an insulating film is formed over one surface of the chip where all the electrodes are formed and a passivation film is formed over the insulating film, and further wherein the protective material on the side walls and a surface of the chip opposite the surface where the electrodes are located have been grinded or polished to a common level, the grinded surface side of the chips opposite the electrodes being secured to a dicing sheet,

wherein at least two of the plurality of chip components are not from a same semiconductor wafer and are pre-tested and determined to be non-defective, and ~~further~~ wherein a flux and a solder bump ~~is~~ are formed on each of said electrodes, there being no electrical conductors on a side of the chip opposite the side where all the electrodes are formed.

Claims 5-7. (Cancelled)

8. (Currently Amended) A pseudo wafer comprising a plurality of same or different electronic chip components each having all electrodes formed on one surface thereof-which are bonded to each other with a protective material coated on side walls therebetween, and wherein there is no protective material located on the one surface of the chip where all the electrodes are formed, wherein the protective material on the side wall and a surface of the chip opposite the surface where the electrodes are located have been grinded or polished to a common level, the grinded surface side of the chips opposite the electrodes being secured to a dicing sheet, and further wherein the plurality of chip components are not originally from a same semiconductor wafer, there being no electrical conductors on a side of the chip opposite the side where all the electrodes are formed, and

wherein an insulating film is formed over the one surface of the chip where all the electrodes are formed and a passivation film is formed over the insulating film, and

wherein the plurality of chip components are pre-tested and determined to be non-defective.

9. (Previously Presented) The pseudo wafer according to claim 8, wherein a solder bump is formed on each of said electrodes.

Claims 10-20. (Cancelled)

Please add the following new claims:

11. (New) The intermediate semiconductor device fabrication structure according to claim 4, wherein each of the plurality of chip components is of a different type.

12. (New) The intermediate semiconductor device fabrication structure according to claim 8, wherein each of the plurality of chip components is of a different type.